Notice of Allowability	Application No.	Applicant(s)	
	09/532,411	ZHANG, KEVIN X.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/25/2005*.

2. ☒ The allowed claim(s) is/are *1-33*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-33, as amended on 11/25/2005 are pending in the instant application. Applicant's arguments have been carefully and fully considered, and are persuasive. Accordingly, the grounds of rejection presented in the office action dated 5/25/2005 have been withdrawn. This application is now in condition for allowance.

Response to Arguments

2. Applicant's arguments, see page 10 lines 11-21, filed 11/25/2005, with respect to claim 1 have been fully considered and are persuasive.

3. **Claim 1** requires "*a pre-decoder coupled with the bit vector replacement circuit to receive a plurality of bit vectors including the second bit vector*". The second bit vector is required by claim 1 to be produced by a bit vector replacement circuit. The replacement control circuit of Takase changes the mapping of the cells in the memory but does not "*substitute a constant bit vector for the first bit vector, in response to the control signal being in a first state, to produce a second bit vector*" the second bit vector being received by a pre-decoder as required by claim 1. The rejection of claims 1-18 has been withdrawn.

4. Applicant's arguments, see page 13 lines 11-16, filed 11/25/2005, with respect to claim 19 have been fully considered and are persuasive.

5. **Claim 19** requires "*a bit vector selection circuit on the die to receive a first bit vector and a control signal, and to select a constant bit vector or the first bit vector responsive to the control signal, and to output the selected bit vector as a second bit*

vector" and "*a decoder circuit on the die coupled to the bit vector selection circuit to receive a plurality of bit vectors including the second bit vector and to combine a subsequence from each of the plurality of bit vectors to identify a wordline corresponding to the plurality of bit vectors*". The decoder circuit of Takase does not "*combine a subsequence from each of the plurality of bit vectors to identify a wordline corresponding to the plurality of bit vectors*" as required by claim 19. The rejection of claims 19-23 has been withdrawn.

6. Applicant's arguments, see page 12 lines 3-9, filed 11/25/2005, with respect to claim 24 have been fully considered and are persuasive.

7. **Claim 24** requires "*means for decoding an address to access a line of the cache memory system responsive to an access request that includes an address represented in a redundant form*" and "*means for decoding an address to access a line of the cache memory system responsive to an access request that includes an address represented in unsigned binary form*". Auslander does not teach or suggest means for decoding an address in a redundant form. The rejection of claim 24 has been withdrawn.

8. Applicant's arguments, see page 11 lines 10-14, filed 11/25/2005, with respect to claim 25 have been fully considered and are persuasive.

9. **Claim 25** as amended requires "*identifying at least in part from the second bit vector and from the first bit vector a word line corresponding to the combined first bit vector and second bit vector*". This is not taught or suggested by Takase. Accordingly, the rejection of claim 25 has been withdrawn.

Reasons for Allowance

10. **Claim 1** recites the limitation "*A bit vector selection circuit on the die to receive a first bit vector and a control signal, and to select a constant bit vector or the first bit vector responsive to the control signal, and to output the selected bit vector as a second bit vector*". This limitation, in combination with the other limitations of the claim is not taught or suggested by the prior art of record.

11. **Claim 19** recites the limitation "*A bit vector selection circuit on the die to receive a first bit vector and a control signal, and to select a constant bit vector or the first bit vector responsive to the control signal, and to output the selected bit vector as a second bit vector*". This limitation, in combination with the other limitations of the claim is not taught or suggested by the prior art of record.

12. **Claim 24** recites the limitations "*Means for decoding an address to access a line of the cache memory system responsive to an access request that includes an address represented in a redundant form*" and "*means for decoding an address to access a line of the cache memory system responsive to an access request that includes an address represented in unsigned binary form*". These limitations in combination are not taught by the prior art of record, and the combination of these decoding means is not suggested by the prior art of record.

13. **Claim 25** recites the limitations "*Setting the second bit vector equal to a constant bit vector if the control signal is in a first state*" and "*Identifying at least in part from the second bit vector and from the first bit vector a word line corresponding to the combined*

first bit vector and second bit vector". These limitations in combination with the other limitations of the claim are not taught or suggested by the prior art of record.

Examiner's Comment

14. Claims 1-33 have been renumbered as follows:

Original numbering	1-24	25	29-33	26-28
New numbering	1-24	30	25-29	31-33

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lynch et al. (US 5,754,819) teach the use of a carry-sum adder to access memory using a redundant form. However, Lynch does not teach or suggest a bit vector replacement circuit as required by claims 1 and 19, means for decoding an address in a redundant form and an unsigned binary form as required by claim 24, or setting the second bit vector equal to a constant bit vector if the control signal is in a first state as required by claim 25.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jared I Rutz
Examiner
Art Unit 2187

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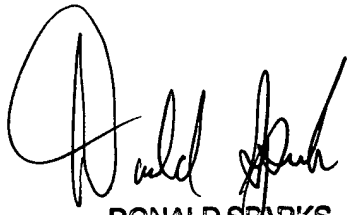

DONALD SPARKS
SUPERVISORY PATENT EXAMINER